REMARKS

This is in response to the Office Action dated July 20, 2006. Claims 1-10 and 15-19 are pending. The Office Action rejects claims 1, 2 and 8 as anticipated by U.S. Patent Publication 2002/0030517 to Kurisu, et al. The Office Action rejects claims 15 and 16 as unpatentable over the Kurisu publication taken in view of U.S. Patent No. 6,041,013 to Kohno. Reexamination and reconsideration are respectfully requested.

The application describes a number of input and output circuits that can implement the JEDEC standard input and output characteristics described in the application. Claim 1 relates for example to the circuit illustrated in FIG. 5, which includes unit circuit having a pull up transistor and two pull down transistors in series. The upper unit circuit includes first and second pull-down transistors TN11 and TN12 connected in series. Because TN11 and TN12 are connected in series, the voltage drop between node C1 and the low voltage supply VSSQ is divided between the two transistors, reducing the voltage drop across each transistor and reducing the stress on the transistors. Reducing the stress on the individual pull-down transistors improves the life of the components of the input and output circuitry.

Resistor R11 is connected between a common node of the unit circuit B1 and the common connecting point C11 and resistor R12 is connected between a common node of the unit circuit B2 and the common connecting point C11. Because two unit circuits are provided with distinct resistors between the unit circuits and the output terminal, output current variations are reduced and there is greater flexibility in designing the performance of the FIG. 5 circuit. In addition, the two resistors provided along the output current path further limit variations on the output current of the circuit.

Claim 1 recites in pertinent part "first resistors formed respectively between said common nodes of said plurality of unit circuits and said common connecting point." The cited Kurisu publication neither teaches nor suggests this limitation.

The Office Action states that the Kurisu publication discloses the presence of plural resistors formed between the output buffer circuit and output terminal. More specifically, the Office Action states that Figure 6 of the publication shows a single resistor L between common node TOUT and output TRV. The referenced single resistor L does not meet the limitation of claim 1, which requires plural resistors, and the single referenced resistor L of Figure 6 further does not meet the positional limitation of claim 1 that requires resistors between the unit circuits' common nodes and the common connecting point for the buffer. In the Figure 6 of the Kurisu publication, TOUT is the common connecting point for the buffer. As shown in that figure of the Kurisu publication, no resistors are present between the common nodes of the plurality of unit circuits and TOUT. The resistor L is positioned outside of the connecting point TOUT and away from the common nodes of the unit circuits.

Thus, the single resistor L of the Kurisu publication, located outside the TOUT node, does not meet the limitation of claim 1 that requires "first resistors formed respectively between said common nodes of said plurality of unit circuits and said common connecting point." Consequently, claim 1 distinguishes over the Kurisu publication and claim 1 and its depending claims 3 and 4 distinguish over the art of record and are in condition for allowance.

Claim 2 relates for example to the circuit illustrated in FIG. 3, which includes first and second unit circuits B1 and B2, each including a pull-up transistor (TP1 and TP2, respectively) and a pull-down transistor (TN1 and TN2, respectively) and each having a common node (C1 and C2, respectively) between their respective pull-

up and pull-down transistors and connected through resistors (R11 and R12, respectively) to a single output terminal (OUT). Because two unit circuits are provided with distinct resistors between the unit circuits and the output terminal, output current variations are reduced and there is greater flexibility in designing the performance of the FIG. 3 circuit.

In addition, the two resistors provided along the output current path further limit variations on the output current of the circuit. This is discussed for the FIG. 3 circuit at page 15, lines 1-8 of the present application. Claim 2 reflects this aspect of the disclosure by reciting, "first resistors formed respectively between said common nodes of said plurality of unit circuits and said common connecting point."

Applicant submits that claim 2 distinguishes over the Kurisu publication by reciting the presence of a plurality of unit circuits, as defined by claim 2, with the common nodes of the plurality of unit circuits connected to the single output terminal through first and second resistors. This is not true of the Kurisu publication. For example, there are not multiple resistors connected to a single output terminal in Figure 6 of the Kurisu publication. Rather, ss shown in that figure of the Kurisu publication, no resistors are present between the common nodes of the plurality of unit circuits and TOUT. In addition, the resistor L is positioned outside of the connecting point TOUT and away from the common nodes of the unit circuits.

Consequently, claim 2 and its dependent claims 5-10 distinguish over the Kurisu publication by reciting "first resistors formed respectively between said common nodes of said plurality of unit circuits and said common connecting point" and are in condition for allowance.

Independent claim 15, in pertinent part, recites "first resistors connected respectively between said common nodes of said plurality of unit circuits and a

common connecting point of said common nodes." This limitation distinguishes over the Kurisu publication for the reasons discussed above with respect to claims 1 and 2. That is, the Kurisu publication does not teach the use of resistors between the common nodes and common connecting points in a buffer circuit as defined by claim 15. As such, claim 15 and its dependent claims 16-19 distinguish over the art of record and are in condition for allowance.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (310) 785-4670 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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